

DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

74HC/HCT4046A **Phase-locked-loop with VCO**

Product specification
Supersedes data of September 1993
File under Integrated Circuits, IC06

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Phase-locked-loop with VCO

74HC/HCT4046A

FEATURES

- Low power consumption
- Centre frequency of up to 17 MHz (typ.) at $V_{CC} = 4.5\text{ V}$
- Choice of three phase comparators: EXCLUSIVE-OR; edge-triggered JK flip-flop; edge-triggered RS flip-flop
- Excellent VCO frequency linearity
- VCO-inhibit control for ON/OFF keying and for low standby power consumption
- Minimal frequency drift
- Operating power supply voltage range: VCO section 3.0 to 6.0 V digital section 2.0 to 6.0 V
- Zero voltage offset due to op-amp buffering
- Output capability: standard
- I_{CC} category: MSI.

GENERAL DESCRIPTION

The 74HC/HCT4046A are high-speed Si-gate CMOS devices and are pin compatible with the "4046" of the "4000B" series. They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT4046A are phase-locked-loop circuits that comprise a linear voltage-controlled oscillator (VCO) and three different phase comparators (PC1, PC2 and PC3) with a common signal input amplifier and a common comparator input.

The signal input can be directly coupled to large voltage signals, or indirectly coupled (with a series capacitor) to small voltage signals. A self-bias input circuit keeps small voltage signals within the linear region of the input amplifiers. With a passive low-pass filter, the "4046A" forms a second-order loop PLL. The excellent VCO linearity is achieved by the use of linear op-amp techniques.

The VCO requires one external capacitor C1 (between C1_A and C1_B) and one external resistor R1 (between R₁ and GND) or two external resistors R1 and R2 (between R₁ and GND, and R₂ and GND). Resistor R1 and capacitor C1 determine the frequency range of the VCO. Resistor R2 enables the VCO to have a frequency offset if required.

The high input impedance of the VCO simplifies the design of low-pass filters by giving the designer a wide choice of resistor/capacitor ranges. In order not to load the low-pass filter, a demodulator output of the VCO input voltage is

provided at pin 10 (DEM_{OUT}). In contrast to conventional techniques where the DEM_{OUT} voltage is one threshold voltage lower than the VCO input voltage, here the DEM_{OUT} voltage equals that of the VCO input. If DEM_{OUT} is used, a load resistor (R_S) should be connected from DEM_{OUT} to GND; if unused, DEM_{OUT} should be left open. The VCO output (VCO_{OUT}) can be connected directly to the comparator input (COMP_{IN}), or connected via a frequency-divider. The VCO output signal has a duty factor of 50% (maximum expected deviation 1%), if the VCO input is held at a constant DC level. A LOW level at the inhibit input (INH) enables the VCO and demodulator, while a HIGH level turns both off to minimize standby power consumption.

The only difference between the HC and HCT versions is the input level specification of the INH input. This input disables the VCO section. The sections of the comparator are identical, so that there is no difference in the SIG_{IN} (pin 14) or COMP_{IN} (pin 3) inputs between the HC and HCT versions.

Phase comparators

The signal input (SIG_{IN}) can be directly coupled to the self-biasing amplifier at pin 14, provided that the signal swing is between the standard HC family input logic levels. Capacitive coupling is required for signals with smaller swings.

Phase comparator 1 (PC1)

This is an EXCLUSIVE-OR network. The signal and comparator input frequencies (f_i) must have a 50% duty factor to obtain the maximum locking range. The transfer characteristic of PC1, assuming ripple ($f_r = 2f_i$) is

suppressed, is: $V_{\text{DEMOUT}} = \frac{V_{CC}}{\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$

where V_{DEMOUT} is the demodulator output at pin 10; $V_{\text{DEMOUT}} = V_{\text{PC1OUT}}$ (via low-pass filter).

The phase comparator gain is: $K_p = \frac{V_{CC}}{\pi} (V/r)$.

The average output voltage from PC1, fed to the VCO input via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of signals (SIG_{IN}) and the comparator input (COMP_{IN}) as shown in Fig.6. The average of V_{DEMOUT} is equal to $\frac{1}{2}V_{CC}$ when there is no signal or noise at SIG_{IN} and with this input the VCO oscillates at the centre frequency (f_0). Typical waveforms for the PC1 loop locked at f_0 are shown in Fig.7.

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The frequency capture range ($2f_c$) is defined as the frequency range of input signals on which the PLL will lock if it was initially out-of-lock. The frequency lock range ($2f_L$) is defined as the frequency range of input signals on which the loop will stay locked if it was initially in lock. The capture range is smaller or equal to the lock range.

With PC1, the capture range depends on the low-pass filter characteristics and can be made as large as the lock range.

This configuration retains lock even with very noisy input signals. Typical behaviour of this type of phase comparator is that it can lock to input frequencies close to the harmonics of the VCO centre frequency.

Phase comparator 2 (PC2)

This is a positive edge-triggered phase and frequency detector. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. PC2 comprises two D-type flip-flops, control-gating and a 3-state output stage. The circuit functions as an up-down counter (Fig.5) where SIG_{IN} causes an up-count and $COMP_{IN}$ a down-count. The transfer function of PC2, assuming ripple ($f_r = f_i$) is suppressed,

$$\text{is: } V_{DEMOUT} = \frac{V_{CC}}{4\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
 $V_{DEMOUT} = V_{PC2OUT}$ (via low-pass filter).

The phase comparator gain is: $K_p = \frac{V_{CC}}{4\pi} (V/r)$.

V_{DEMOUT} is the resultant of the initial phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig.8. Typical waveforms for the PC2 loop locked at f_o are shown in Fig.9.

When the frequencies of SIG_{IN} and $COMP_{IN}$ are equal but the phase of SIG_{IN} leads that of $COMP_{IN}$, the p-type output driver at $PC2_{OUT}$ is held "ON" for a time corresponding to the phase difference (ϕ_{DEMOUT}). When the phase of SIG_{IN} lags that of $COMP_{IN}$, the n-type driver is held "ON".

When the frequency of SIG_{IN} is higher than that of $COMP_{IN}$, the p-type output driver is held "ON" for most of the input signal cycle time, and for the remainder of the cycle both n and p-type drivers are "OFF" (3-state). If the SIG_{IN} frequency is lower than the $COMP_{IN}$ frequency, then it is the n-type driver that is held "ON" for most of the cycle. Subsequently, the voltage at the capacitor (C2) of the low-pass filter connected to $PC2_{OUT}$ varies until the signal

and comparator inputs are equal in both phase and frequency. At this stable point the voltage on C2 remains constant as the PC2 output is in 3-state and the VCO input at pin 9 is a high impedance. Also in this condition, the signal at the phase comparator pulse output (PCP_{OUT}) is a HIGH level and so can be used for indicating a locked condition.

Thus, for PC2, no phase difference exists between SIG_{IN} and $COMP_{IN}$ over the full frequency range of the VCO. Moreover, the power dissipation due to the low-pass filter is reduced because both p and n-type drivers are "OFF" for most of the signal input cycle. It should be noted that the PLL lock range for this type of phase comparator is equal to the capture range and is independent of the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC2, to its lowest frequency.

Phase comparator 3 (PC3)

This is a positive edge-triggered sequential phase detector using an RS-type flip-flop. When the PLL is using this comparator, the loop is controlled by positive signal transitions and the duty factors of SIG_{IN} and $COMP_{IN}$ are not important. The transfer characteristic of PC3, assuming ripple ($f_r = f_i$) is suppressed,

$$\text{is: } V_{DEMOUT} = \frac{V_{CC}}{2\pi} (\phi_{SIGIN} - \phi_{COMPIN})$$

where V_{DEMOUT} is the demodulator output at pin 10;
 $V_{DEMOUT} = V_{PC3OUT}$ (via low-pass filter).

The phase comparator gain is: $K_p = \frac{V_{CC}}{2\pi} (V/r)$.

The average output from PC3, fed to the VCO via the low-pass filter and seen at the demodulator output at pin 10 (V_{DEMOUT}), is the resultant of the phase differences of SIG_{IN} and $COMP_{IN}$ as shown in Fig.10. Typical waveforms for the PC3 loop locked at f_o are shown in Fig.11.

The phase-to-output response characteristic of PC3 (Fig.10) differs from that of PC2 in that the phase angle between SIG_{IN} and $COMP_{IN}$ varies between 0° and 360° and is 180° at the centre frequency. Also PC3 gives a greater voltage swing than PC2 for input phase differences but as a consequence the ripple content of the VCO input signal is higher. The PLL lock range for this type of phase comparator and the capture range are dependent on the low-pass filter. With no signal present at SIG_{IN} the VCO adjusts, via PC3, to its lowest frequency.

Phase-locked-loop with VCO

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QUICK REFERENCE DATAGND = 0 V; T_{amb} = 25 °C

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
f _o	VCO centre frequency	C1 = 40 pF; R1 = 3 kΩ; V _{CC} = 5 V	19	19	MHz
C _I	input capacitance (pin 5)		3.5	3.5	pF
C _{PD}	power dissipation capacitance per package	notes 1 and 2	24	24	pF

Notes

- C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
where:
f_i = input frequency in MHz.
f_o = output frequency in MHz.
C_L = output load capacitance in pF.
V_{CC} = supply voltage in V.
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
- Applies to the phase comparator section only (VCO disabled). For power dissipation of the VCO and demodulator sections see Figs 22, 23 and 24.

ORDERING INFORMATIONSee *"74HC/HCT/HCU/HCMOS Logic Package Information"*.**APPLICATIONS**

- FM modulation and demodulation
- Frequency synthesis and multiplication
- Frequency discrimination
- Tone decoding
- Data synchronization and conditioning
- Voltage-to-frequency conversion
- Motor-speed control.

PACKAGE OUTLINESSee *"74HC/HCT/HCU/HCMOS Logic Package Outlines"*.

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PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	PCP _{OUT}	phase comparator pulse output
2	PC1 _{OUT}	phase comparator 1 output
3	COMP _{IN}	comparator input
4	VCO _{OUT}	VCO output
5	INH	inhibit input
6	C1 _A	capacitor C1 connection A
7	C1 _B	capacitor C1 connection B
8	GND	ground (0 V)
9	VCO _{IN}	VCO input
10	DEM _{OUT}	demodulator output
11	R ₁	resistor R1 connection
12	R ₂	resistor R2 connection
13	PC2 _{OUT}	phase comparator 2 output
14	SIG _{IN}	signal input
15	PC3 _{OUT}	phase comparator 3 output
16	V _{CC}	positive supply voltage

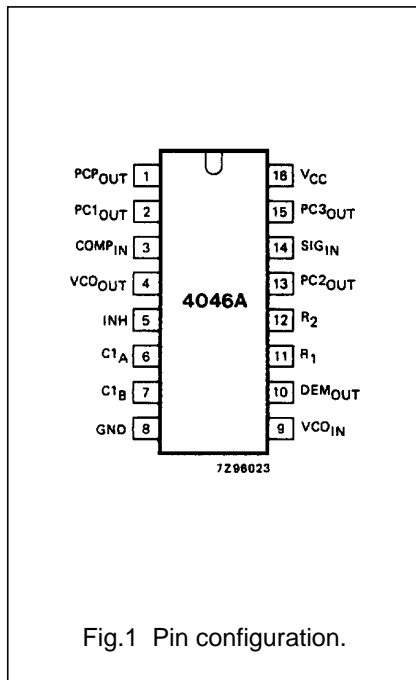


Fig.1 Pin configuration.

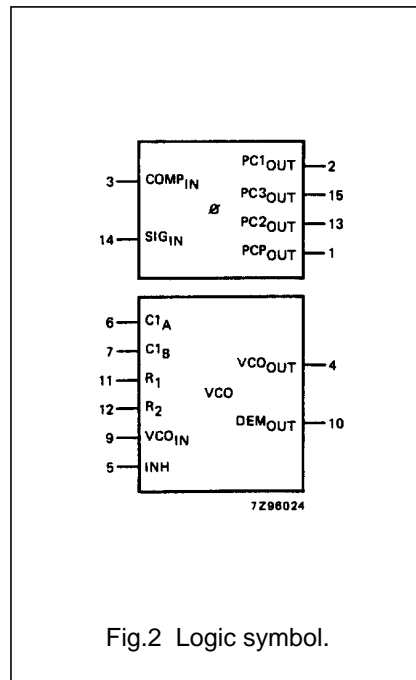


Fig.2 Logic symbol.

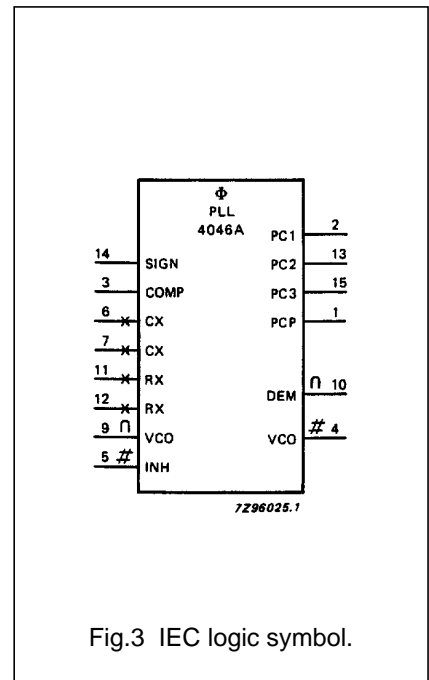
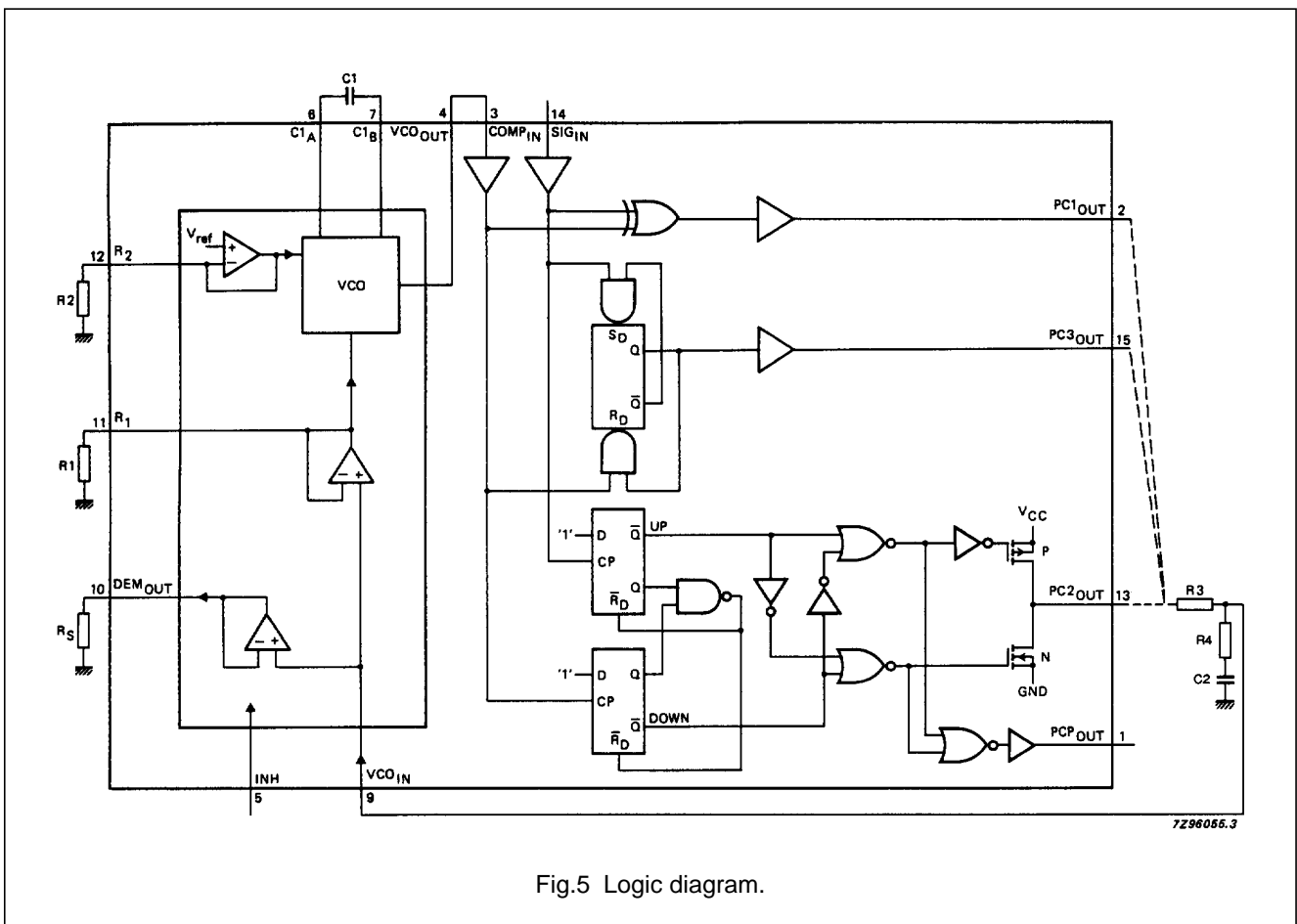
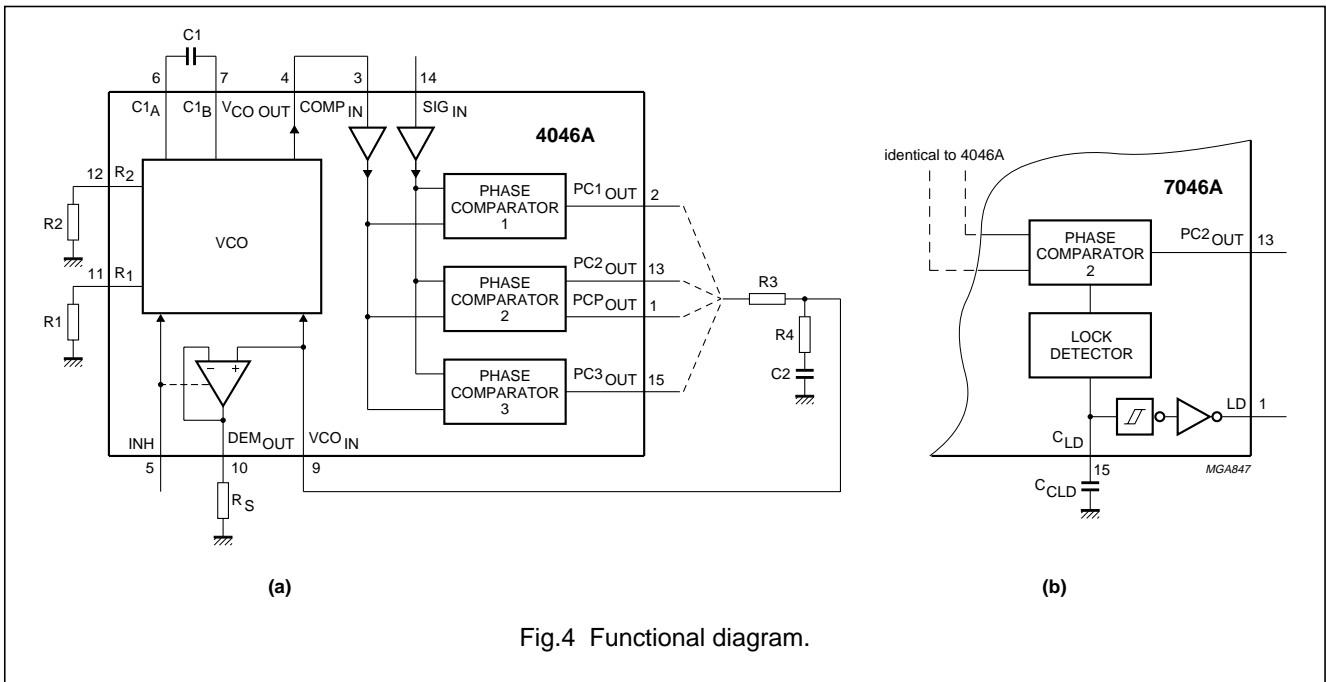


Fig.3 IEC logic symbol.

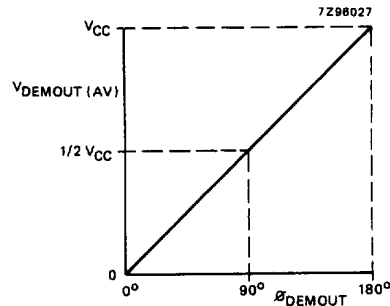
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$$V_{\text{DEMOUT}} = V_{\text{PC2OUT}} = \frac{V_{\text{CC}}}{\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

$$\phi_{\text{DEMOUT}} = (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}}).$$

Fig.6 Phase comparator 1: average output voltage versus input phase difference.

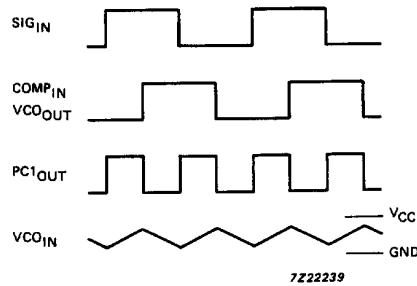
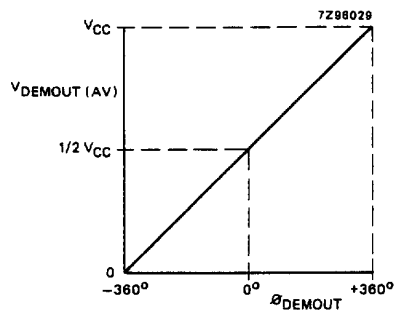


Fig.7 Typical waveforms for PLL using phase comparator 1, loop locked at f_0 .



$$V_{\text{DEMOUT}} = V_{\text{PC2OUT}} = \frac{V_{\text{CC}}}{4\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

$$\phi_{\text{DEMOUT}} = (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}}).$$

Fig.8 Phase comparator 2: average output voltage versus input phase difference.

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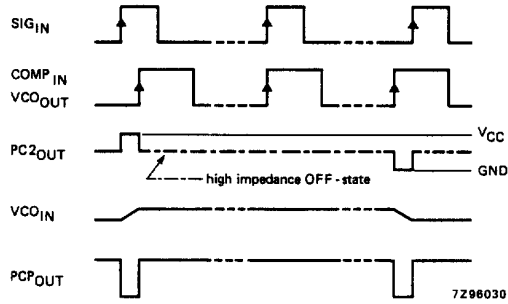
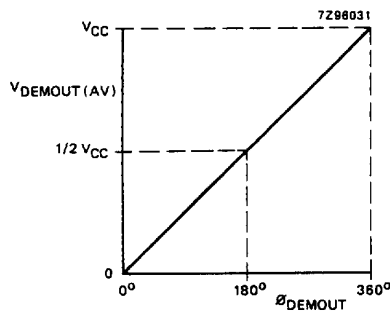


Fig.9 Typical waveforms for PLL using phase comparator 2, loop locked at f_o .



$$V_{\text{DEMOUT}} = V_{\text{PC3OUT}} = \frac{V_{\text{CC}}}{2\pi} (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

$$\phi_{\text{DEMOUT}} = (\phi_{\text{SIGIN}} - \phi_{\text{COMPIN}})$$

Fig.10 Phase comparator 3: average output voltage versus input phase difference:

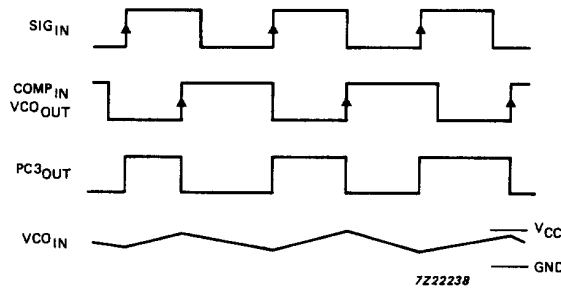


Fig.11 Typical waveforms for PLL using phase comparator 3, loop locked at f_o .

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RECOMMENDED OPERATING CONDITIONS FOR 74HC/HCT

SYMBOL	PARAMETER	74HC			74HCT			UNIT	CONDITIONS
		min.	typ.	max.	min.	typ.	max.		
V _{CC}	DC supply voltage	3.0	5.0	6.0	4.5	5.0	5.5	V	
V _{CC}	DC supply voltage if VCO section is not used	2.0	5.0	6.0	4.5	5.0	5.5	V	
V _I	DC input voltage range	0		V _{CC}	0		V _{CC}	V	
V _O	DC output voltage range	0		V _{CC}	0		V _{CC}	V	
T _{amb}	operating ambient temperature range	-40		+85	-40		+85	°C	see DC and AC CHARACTERISTICS
T _{amb}	operating ambient temperature range	-40		+125	-40		+125	°C	
t _r , t _f	input rise and fall times (pin 5)		6.0	1000		6.0	500	ns	V _{CC} = 2.0 V
			6.0	500		6.0	500	ns	V _{CC} = 4.5 V
			6.0	400		6.0	500	ns	V _{CC} = 6.0 V

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	CONDITIONS
V _{CC}	DC supply voltage	-0.5	+7	V	
±I _{IK}	DC input diode current		20	mA	for V _I < -0.5 V or V _I > V _{CC} + 0.5 V
±I _{OK}	DC output diode current		20	mA	for V _O < -0.5 V or V _O > V _{CC} + 0.5 V
±I _O	DC output source or sink current		25	mA	for -0.5 V < V _O < V _{CC} + 0.5 V
±I _{CC} ; ±I _{GND}	DC V _{CC} or GND current		50	mA	
T _{stg}	storage temperature range	-65	+150	°C	
P _{tot}	power dissipation per package				for temperature range: - 40 to +125 °C 74HC/HCT
	plastic DIL		750	mW	above + 70 °C: derate linearly with 12 mW/K
	plastic mini-pack (SO)		500	mW	above + 70 °C: derate linearly with 8 mW/K

Phase-locked-loop with VCO

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DC CHARACTERISTICS FOR 74HC

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS	
		74HC									V _{CC} (V)	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
I _{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	µA	6.0	pins 3, 5, and 14 at V _{CC} ; pin 9 at GND; I _I at pins 3 and 14 to be excluded	

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYM-BOL	PARAMETER	T _{amb} (°C)								UNIT	TEST CONDITIONS		
		74HC									V _{CC} (V)	V _I	OTHER
		+25			-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.					
V _{IH}	DC coupled HIGH level input voltage SIG _{IN} , COMP _{IN}	1.5	1.2		1.5		1.5		V	2.0			
		3.15	2.4		3.15		3.15			4.5			
		4.2	3.2		4.2		4.2			6.0			
V _{IL}	DC coupled LOW level input voltage SIG _{IN} , COMP _{IN}		0.8	0.5		0.5		0.5	V	2.0			
			2.1	1.35		1.35		1.35		4.5			
			2.8	1.8		1.8		1.8		6.0			
V _{OH}	HIGH level output voltage PCP _{OUT} , PC _n OUT	1.9	2.0		1.9		1.9		V	2.0	V _{IH} or V _{IL}	-I _O = 20 µA	
		4.4	4.5		4.4		4.4			4.5		-I _O = 20 µA	
		5.9	6.0		5.9		5.9			6.0		-I _O = 20 µA	
V _{OH}	HIGH level output voltage PCP _{OUT} , PC _n OUT	3.98	4.32		3.84		3.7		V	4.5	V _{IH} or V _{IL}	-I _O = 4.0 mA	
		5.48	5.81		5.34		5.2			6.0		-I _O = 5.2 mA	
V _{OL}	LOW level output voltage PCP _{OUT} , PC _n OUT		0	0.1		0.1		0.1	V	2.0	V _{IH} or V _{IL}	I _O = 20 µA	
			0	0.1		0.1		0.1		4.5		I _O = 20 µA	
			0	0.1		0.1		0.1		6.0		I _O = 20 µA	
V _{OL}	LOW level output voltage PCP _{OUT} , PC _n OUT		0.15	0.26		0.33		0.4	V	4.5	V _{IH} or V _{IL}	I _O = 4.0 mA	
			0.16	0.26		0.33		0.4		6.0		I _O = 5.2 mA	
±I _I	input leakage current SIG _{IN} , COMP _{IN}			3.0		4.0		5.0	µA	2.0	V _{CC} or GND		
				7.0		9.0		11.0		3.0			
				18.0		23.0		27.0		4.5			
				30.0		38.0		45.0		6.0			
±I _{OZ}	3-state OFF-state current PC2 _{OUT}			0.5		5.0		10.0	µA	6.0	V _{IH} or V _{IL}	V _O = V _{CC} or GND	

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SYM-BOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} (V)	V _I	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
R _I	input resistance SIG _{IN} , COMP _{IN}		800 250 150					kΩ kΩ kΩ	3.0 4.5 6.0	V _I at self-bias operating point; Δ V _I = 0.5 V; see Figs 12, 13 and 14		

VCO section

Voltages are referenced to GND (ground = 0 V)

SYM-BOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} (V)	V _I	OTHER	
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.					max.
V _{IH}	HIGH level input voltage INH	2.1 3.15 4.2	1.7 2.4 3.2		2.1 3.15 4.2		2.1 3.15 4.2	V	3.0 4.5 6.0			
V _{IL}	LOW level input voltage INH		1.3 2.1 2.8	0.9 1.35 1.8		0.9 1.35 1.8	0.9 1.35 1.8	V	3.0 4.5 6.0			
V _{OH}	HIGH level output voltage VCO _{OUT}	2.9 4.4 5.9	3.0 4.5 6.0		2.9 4.4 5.9		2.9 4.4 5.9	V	3.0 4.5 6.0	V _{IH} or V _{IL}	-I _O = 20 μA -I _O = 20 μA -I _O = 20 μA	
V _{OH}	HIGH level output voltage VCO _{OUT}	3.98 5.48	4.32 5.81		3.84 5.34		3.7 5.2	V	4.5 6.0	V _{IH} or V _{IL}	-I _O = 4.0 mA -I _O = 5.2 mA	
V _{OL}	LOW level output voltage VCO _{OUT}		0 0 0	0.1 0.1 0.1		0.1 0.1 0.1	0.1 0.1 0.1	V	3.0 4.5 6.0	V _{IH} or V _{IL}	I _O = 20 μA I _O = 20 μA I _O = 20 μA	
V _{OL}	LOW level output voltage VCO _{OUT}		0.15 0.16	0.26 0.26		0.33 0.33	0.4 0.4	V	4.5 6.0	V _{IH} or V _{IL}	I _O = 4.0 mA I _O = 5.2 mA	
V _{OL}	LOW level output voltage C1 _A , C1 _B			0.40 0.40		0.47 0.47	0.54 0.54	V	4.5 6.0	V _{IH} or V _{IL}	I _O = 4.0 mA I _O = 5.2 mA	
±I _I	input leakage current INH, VCO _{IN}			0.1		1.0	1.0	μA	6.0	V _{CC} or GND		
R1	resistor range	3.0 3.0 3.0		300 300 300				kΩ	3.0 4.5 6.0		note 1	

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SYM-BOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HC								V _{CC} (V)	V _I	OTHER
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
R ₂	resistor range	3.0		300					kΩ	3.0 4.5 6.0	note 1	
C1	capacitor range	40		no limit					pF	3.0 4.5 6.0		
V _{VCOIN}	operating voltage range at VCO _{IN}	1.1		1.9					V	3.0 4.5 6.0	over the range specified for R1; for linearity see Figs 20 and 21	

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/ or R2 are/is > 10 kΩ.

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V _{CC} V	OTHER
		+25			-40 to+85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R _S	resistor range	50		300					kΩ	3.0 4.5 6.0	at R _S > 300 kΩ the leakage current can influence V _{DEMOUT}
V _{OFF}	offset voltage VCO _{IN} to V _{DEMOUT}		±30 ±20 ±10						mV	3.0 4.5 6.0	V _I = V _{VCOIN} = 1/2 V _{CC} ; values taken over R _S range; see Fig.15
R _D	dynamic output resistance at DEM _{OUT}		25 25 25						Ω	3.0 4.5 6.0	V _{DEMOUT} = 1/2 V _{CC}

Phase-locked-loop with VCO

74HC/HCT4046A

AC CHARACTERISTICS FOR 74HC

Phase comparator section

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS			
		74HC							V _{CC} (V)	OTHER		
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.				max.	
t _{PHL} / t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PC1 _{OUT}		63	200		250		300	ns	2.0	Fig.16	
			23	40		50		60				
			18	34		43		51				
t _{PHL} / t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PCP _{OUT}		96	340		425		510	ns	2.0	Fig.16	
			35	68		85		102				
			28	58		72		87				
t _{PHL} / t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PC3 _{OUT}		77	270		340		405	ns	2.0	Fig.16	
			28	54		68		81				
			22	46		58		69				
t _{PZH} / t _{PZL}	3-state output enable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		83	280		350		420	ns	2.0	Fig.17	
			30	56		70		84				
			24	48		60		71				
t _{PHZ} / t _{PLZ}	3-state output disable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		99	325		405		490	ns	2.0	Fig.17	
			36	65		81		98				
			29	55		69		83				
t _{THL} / t _{TLH}	output transition time		19	75		95		110	ns	2.0	Fig.16	
			7	15		19		22				
			6	13		16		19				
V _{I(p-p)}	AC coupled input sensitivity (peak-to-peak value) at SIG _{IN} or COMP _{IN}		9						mV	2.0	f _i = 1 MHz	
			11									
			15									
			33									

Phase-locked-loop with VCO

74HC/HCT4046A

VCO section

GND = 0 V; $t_r = t_f = 6$ ns; $C_L = 50$ pF

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	typ.	max.	min.	max.			
$\Delta f/T$	frequency stability with temperature change				0.20 0.15 0.14				%/K	3.0 4.5 6.0	$V_I = V_{VCOIN} = 1/2 V_{CC}$; $R1 = 100$ k Ω ; $R2 = \infty$; $C1 = 100$ pF; see Fig.18
f_o	VCO centre frequency (duty factor = 50%)	7.0 11.0 13.0	10.0 17.0 21.0						MHz	3.0 4.5 6.0	$V_{VCOIN} = 1/2 V_{CC}$; $R1 = 3$ k Ω ; $R2 = \infty$; $C1 = 40$ pF; see Fig.19
Δf_{VCO}	VCO frequency linearity		1.0 0.4 0.3						%	3.0 4.5 6.0	$R1 = 100$ k Ω ; $R2 = \infty$; $C1 = 100$ pF; see Figs 20 and 21
δ_{VCO}	duty factor at V_{COOUT}		50 50 50						%	3.0 4.5 6.0	

DC CHARACTERISTICS FOR 74HCT

Quiescent supply current

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V_{CC} (V)	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
I_{CC}	quiescent supply current (VCO disabled)			8.0		80.0		160.0	μ A	6.0	pins 3, 5 and 14 at V_{CC} ; pin 9 at GND; I_I at pins 3 and 14 to be excluded
ΔI_{CC}	additional quiescent supply current per input pin for unit load coefficient is 1 (note 1) $V_I = V_{CC} - 2.1$ V		100	360		450		490	μ A	4.5 to 5.5	pins 3 and 14 at V_{CC} ; pin 9 at GND; I_I at pins 3 and 14 to be excluded

Note

- The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given above. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
INH	1.00

Phase-locked-loop with VCO

74HC/HCT4046A

DC CHARACTERISTICS FOR 74HCT

Phase comparator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V _{CC} (V)	V _I	OTHER
		+25			-40 to +85		-40 to +125					
		min	typ.	max	min	max	min.	max.				
V _{IH}	DC coupled HIGH level input voltage SIG _{IN} , COMP _{IN}	3.15	2.4						V	4.5		
V _{IL}	DC coupled LOW level input voltage SIG _{IN} , COMP _{IN}		2.1	1.35					V	4.5		
V _{OH}	HIGH level output voltage PCP _{OUT} , PC _n OUT	4.4	4.5		4.4		4.4		V	4.5	V _{IH} or V _{IL}	-I _O = 20 µA
V _{OH}	HIGH level output voltage PCP _{OUT} , PC _n OUT	3.98	4.32		3.84		3.7		V	4.5	V _{IH} or V _{IL}	-I _O = 4.0 mA
V _{OL}	LOW level output voltage PCP _{OUT} , PC _n OUT		0	0.1		0.1		0.1	V	4.5	V _{IH} or V _{IL}	I _O = 20 µA
V _{OL}	LOW level output voltage PCP _{OUT} , PC _n OUT		0.15	0.26		0.33		0.4	V	4.5	V _{IH} or V _{IL}	I _O = 4.0 mA
±I _I	input leakage current SIG _{IN} , COMP _{IN}			30		38		45	µA	5.5	V _{CC} or GN D	
±I _{OZ}	3-state OFF-state current PC2 _{OUT}			0.5		5.0		10.0	µA	5.5	V _{IH} or V _{IL}	V _O = V _{CC} or GND
R _I	input resistance SIG _{IN} , COMP _{in}		250						kΩ	4.5	V _I at self-bias operating point; Δ V _I = 0.5 V; see Figs 12, 13 and 14	

Phase-locked-loop with VCO

74HC/HCT4046A

DC CHARACTERISTICS FOR 74HCT

VCO section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS		
		74HCT								V _{CC} (V)	V _I	OTHER
		+25			-40 to +85		-40 to +125					
		min	typ.	max	min	max	min.	max.				
V _{IH}	HIGH level input voltage INH	2.0	1.6		2.0		2.0		V	4.5 to 5.5		
V _{IL}	LOW level input voltage INH		1.2	0.8		0.8		0.8	V	4.5 to 5.5		
V _{OH}	HIGH level output voltage VCO _{OUT}	4.4	4.5		4.4		4.4		V	4.5	V _{IH} or V _{IL}	-I _O = 20 µA
V _{OH}	HIGH level output voltage VCO _{OUT}	3.98	4.32		3.84		3.7		V	4.5	V _{IH} or V _{IL}	-I _O = 4.0 mA
V _{OL}	LOW level output voltage VCO _{OUT}		0	0.1		0.1		0.1	V	4.5	V _{IH} or V _{IL}	I _O = 20 µA
V _{OL}	LOW level output voltage VCO _{OUT}		0.15	0.26		0.33		0.4	V	4.5	V _{IH} or V _{IL}	I _O = 4.0 mA
V _{OL}	LOW level output voltage C1 _A , C1 _B (test purposes only)			0.40		0.47		0.54	V	4.5	V _{IH} or V _{IL}	I _O = 4.0 mA
±I _I	input leakage current INH, VCO _{IN}			0.1		1.0		1.0	µA	5.5	V _{CC} or GND	
R1	resistor range	3.0		300					kΩ	4.5		note 1
R ₂	resistor range	3.0		300					kΩ	4.5		note 1
C1	capacitor range	40		no limit					pF	4.5		
V _{VCOIN}	operating voltage range at VCO _{IN}	1.1		3.4					V	4.5		over the range specified for R1; for linearity see Figs 20 and 21

Note

1. The parallel value of R1 and R2 should be more than 2.7 kΩ. Optimum performance is achieved when R1 and/or R2 are/is > 10 kΩ.

Phase-locked-loop with VCO

74HC/HCT4046A

DC CHARACTERISTICS FOR 74HCT

Demodulator section

Voltages are referenced to GND (ground = 0 V)

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
R _S	resistor range	50		300					kΩ	4.5	at R _S > 300 kΩ the leakage current can influence V _{DEMOUT}
V _{OFF}	offset voltage VCO _{IN} to V _{DEMOUT}		±20						mV	4.5	V _I = V _{VCOIN} = 1/2 V _{CC} ; values taken over R _S range; see Fig.15
R _D	dynamic output resistance at DEM _{OUT}		25						Ω	4.5	V _{DEMOUT} = 1/2 V _{CC}

AC CHARACTERISTICS FOR 74HCT

Phase comparator section

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)							UNIT	TEST CONDITIONS	
		74HCT								V _{CC} (V)	OTHER
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t _{PHL} / t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PC1 _{OUT}		23	40		50		60	ns	4.5	Fig.16
t _{PHL} / t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PCP _{OUT}		35	68		85		102	ns	4.5	Fig.16
t _{PHL} / t _{PLH}	propagation delay SIG _{IN} , COMP _{IN} to PC3 _{OUT}		28	54		68		81	ns	4.5	Fig.16
t _{PZH} / t _{PZL}	3-state output enable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		30	56		70		84	ns	4.5	Fig.17

Phase-locked-loop with VCO

74HC/HCT4046A

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
t _{PHZ} / t _{PLZ}	3-state output disable time SIG _{IN} , COMP _{IN} to PC2 _{OUT}		36	65		81		98	ns	4.5	Fig.17
t _{THL} / t _{TLH}	output transition time		7	15		19		22	ns	4.5	Fig.16
V _{I (p-p)}	AC coupled input sensitivity (peak-to-peak value) at SIG _{IN} or COMP _{IN}		15						mV	4.5	f _i = 1 MHz

VCO section

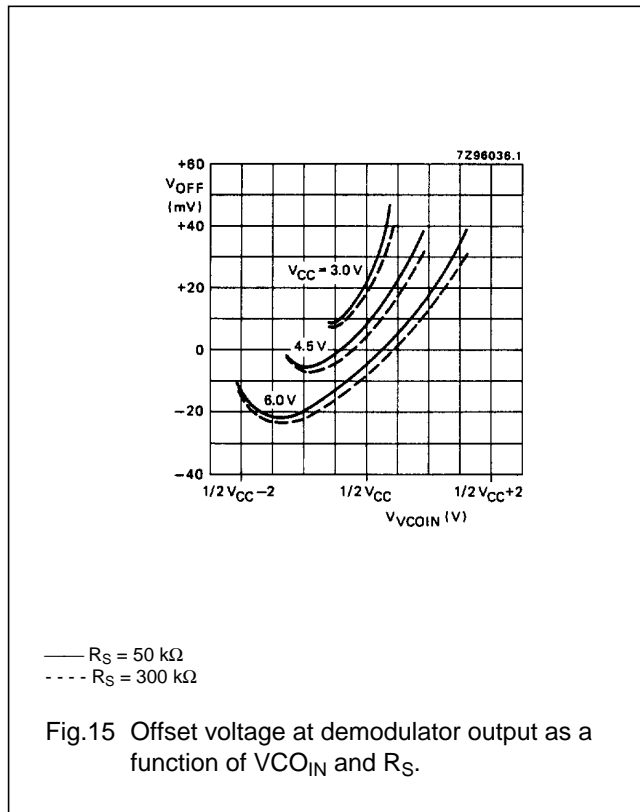
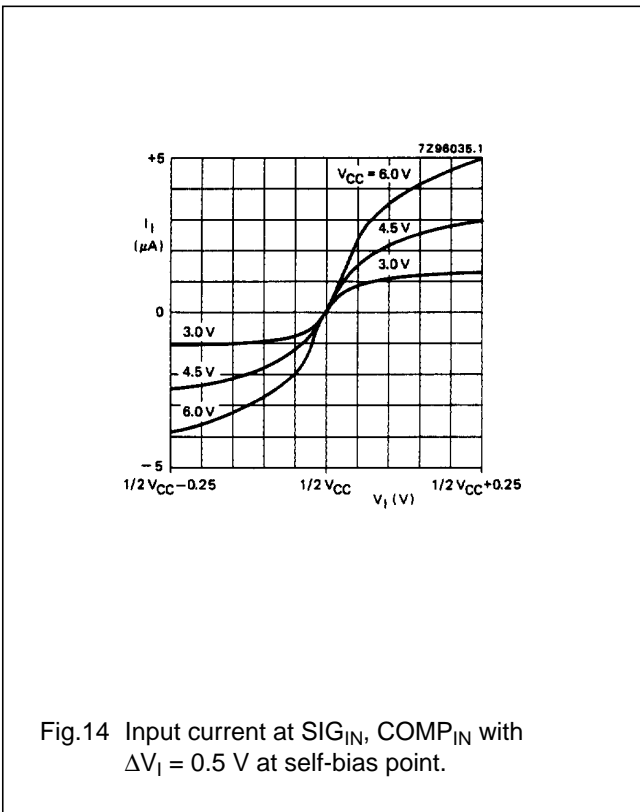
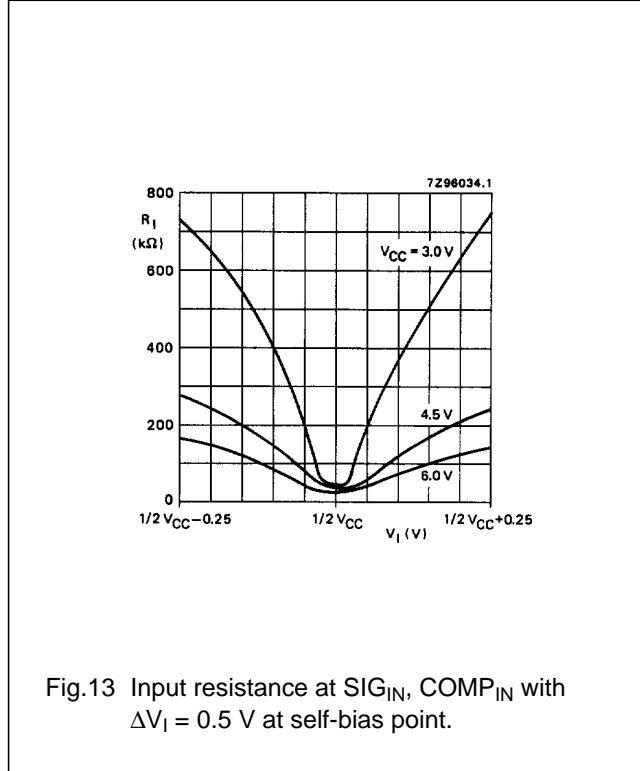
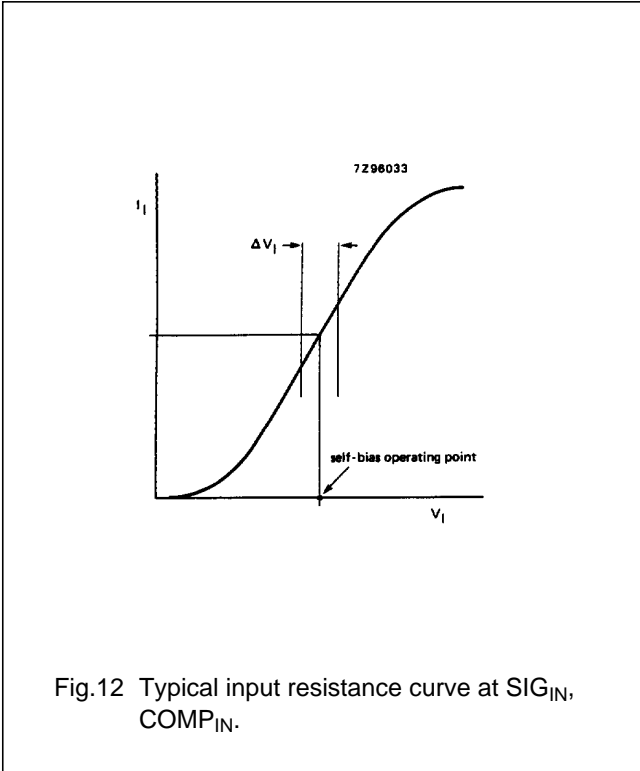
GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

SYMBOL	PARAMETER	T _{amb} (°C)						UNIT	TEST CONDITIONS		
		74HCT							V _{CC} (V)	OTHER	
		+25			-40 to +85		-40 to +125				
		min.	typ.	max.	min.	max.	min.				max.
Δf/T	frequency stability with temperature change				0.15				%/K	4.5	V _I = V _{VCOIN} within recommended range; R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Fig.18b
f _o	VCO centre frequency (duty factor = 50%)	11.0	17.0						MHz	4.5	V _{VCOIN} = 1/2 V _{CC} ; R1 = 3 kΩ; R2 = ∞; C1 = 40 pF; see Fig.19
Δf _{VCO}	VCO frequency linearity		0.4						%	4.5	R1 = 100 kΩ; R2 = ∞; C1 = 100 pF; see Figs 20 and 21
δ _{VCO}	duty factor at VCO _{OUT}		50						%	4.5	

Phase-locked-loop with VCO

74HC/HCT4046A

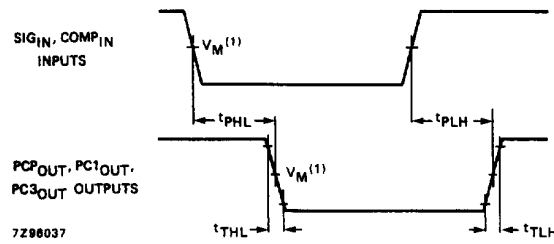
FIGURE REFERENCES FOR DC CHARACTERISTICS



Phase-locked-loop with VCO

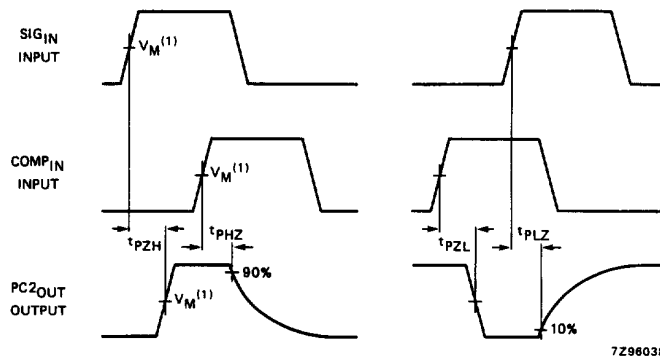
74HC/HCT4046A

AC WAVEFORMS



(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$

Fig.16 Waveforms showing input (SIG_{IN}, COMP_{IN}) to output (PCP_{OUT}, PC1_{OUT}, PC3_{OUT}) propagation delays and the output transition times.

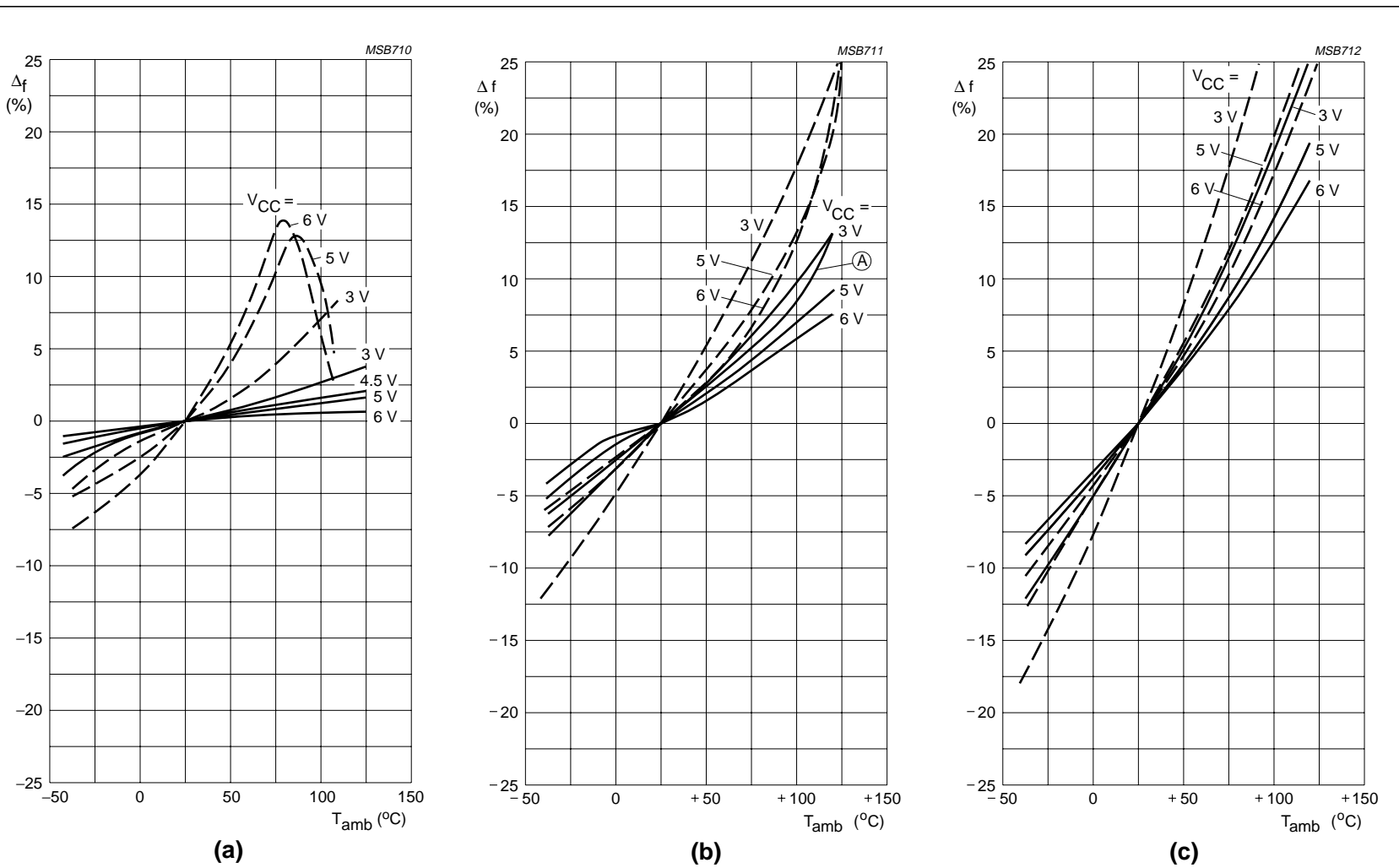


(1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$

Fig.17 Waveforms showing the 3-state enable and disable times for PC2_{OUT}.

Phase-locked-loop with VCO

74HC/HCT4046A



To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

Fig.18 Frequency stability of the VCO as a function of ambient temperature with supply voltage as a parameter.

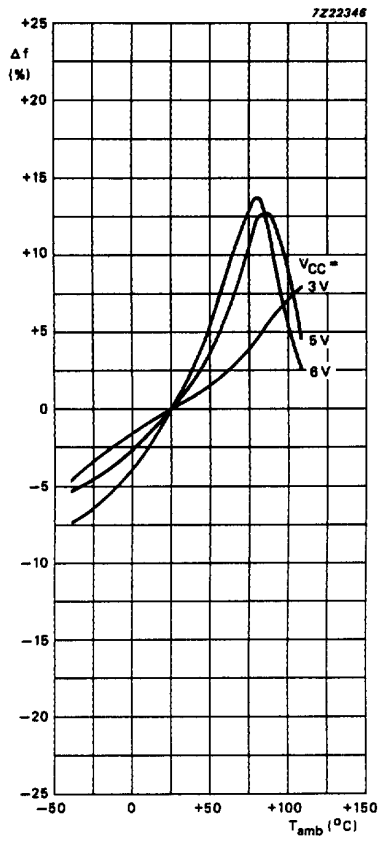
— without offset ($R_2 = \infty$): (a) $R_1 = 3\text{ k}\Omega$; (b) $R_1 = 10\text{ k}\Omega$; (c) $R_1 = 300\text{ k}\Omega$.

- - - with offset ($R_1 = \infty$): (a) $R_2 = 3\text{ k}\Omega$; (b) $R_2 = 10\text{ k}\Omega$; (c) $R_2 = 300\text{ k}\Omega$.

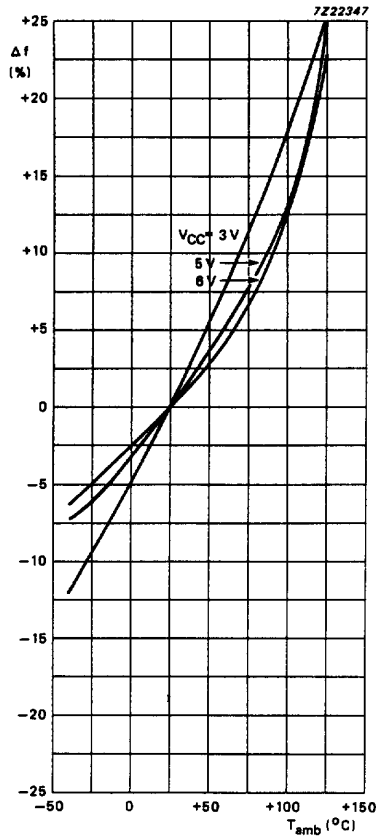
In (b), the frequency stability for $R_1 = R_2 = 10\text{ k}\Omega$ at 5 V is also given (curve A). This curve is set by the total VCO bias current, and is not simply the addition of the two 10 k Ω stability curves. $C_1 = 100\text{ pF}$; $V_{VCO\text{ IN}} = 0.5 V_{CC}$.

Phase-locked-loop with VCO

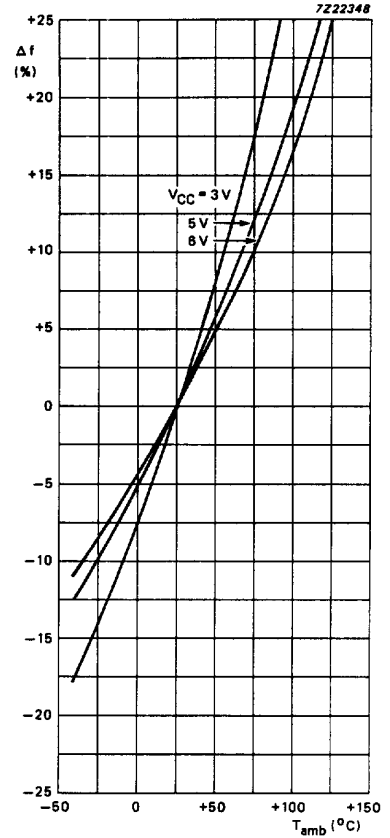
74HC/HCT4046A



(d) $R_2 = 3 \text{ k}\Omega$
 $R_1 = \infty$



(e) $R_2 = 10 \text{ k}\Omega$
 $R_1 = \infty$



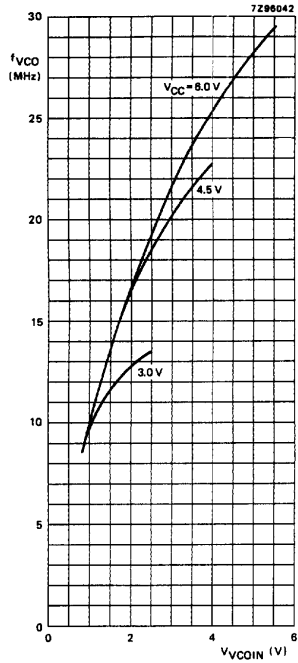
(f) $R_2 = 300 \text{ k}\Omega$
 $R_1 = \infty$

To obtain optimum temperature stability, C1 must be as small as possible but larger than 100 pF.

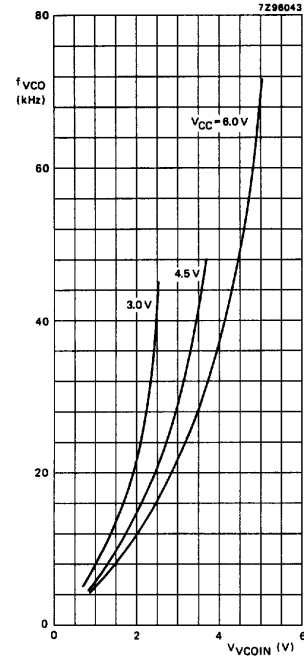
Fig.18 Continued.

Phase-locked-loop with VCO

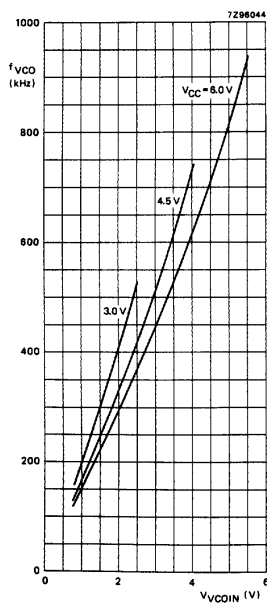
74HC/HCT4046A



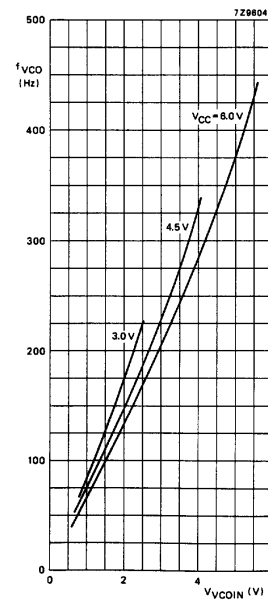
(a) $R_1 = 3 \text{ k}\Omega$;
 $C_1 = 40 \text{ pF}$



(b) $R_1 = 3 \text{ k}\Omega$;
 $C_1 = 100 \text{ nF}$



(c) $R_1 = 300 \text{ k}\Omega$;
 $C_1 = 40 \text{ pF}$



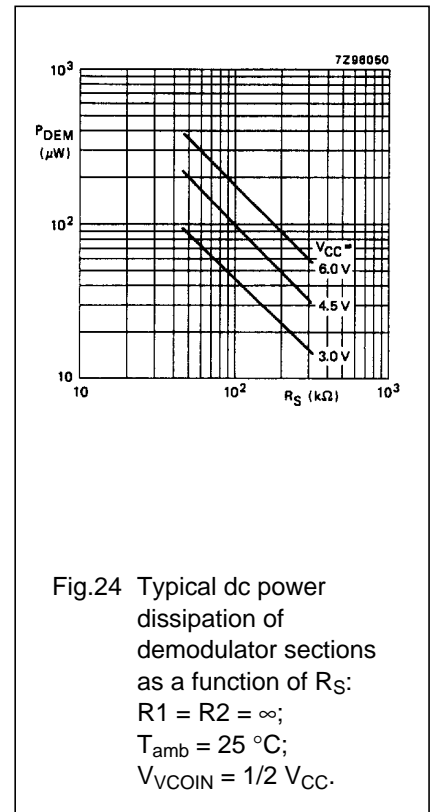
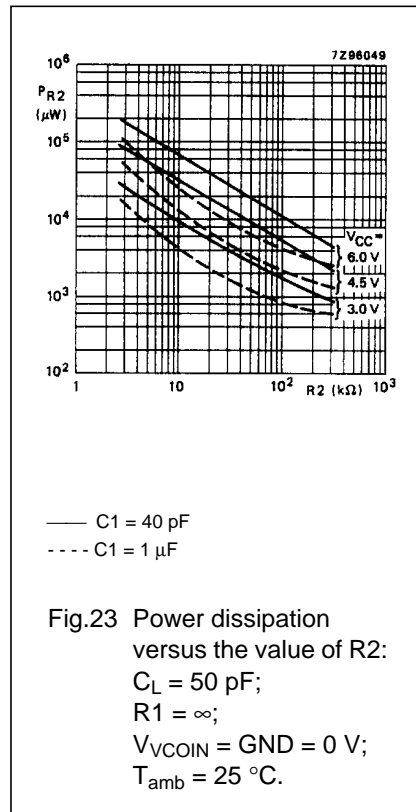
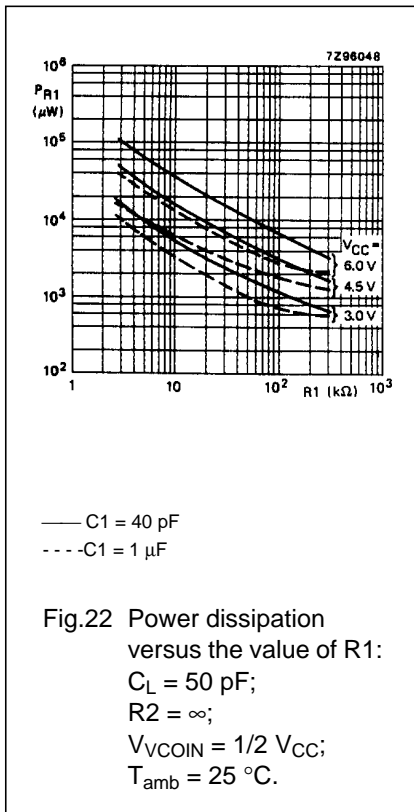
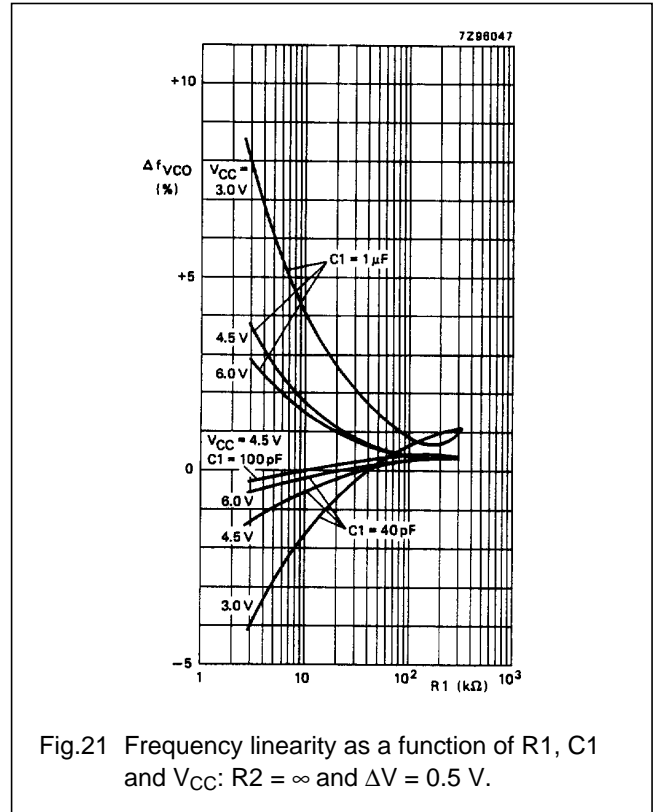
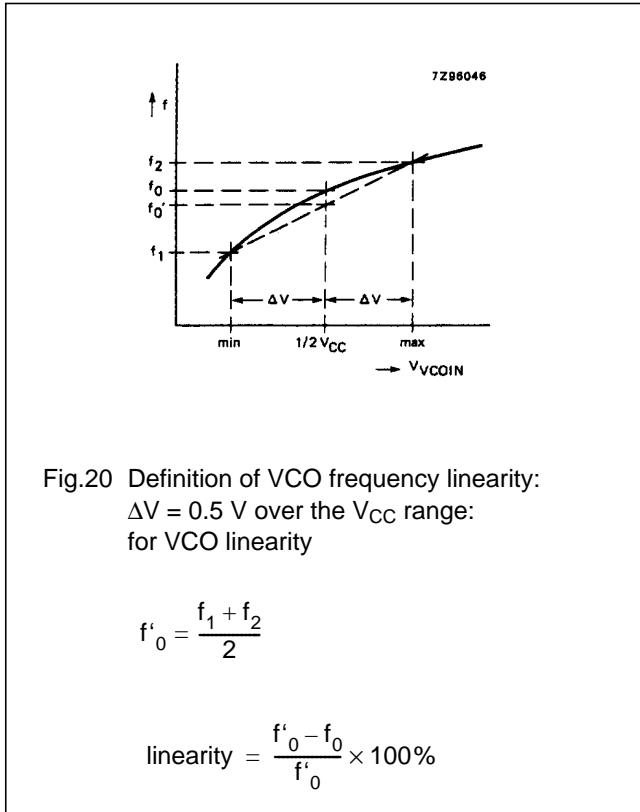
(d) $R_1 = 300 \text{ k}\Omega$;
 $C_1 = 100 \text{ nF}$

To obtain optimum temperature stability, C_1 must be as small as possible but larger than 100 pF.

Fig.19 Graphs showing VCO frequency (f_{VCO}) as a function of the VCO input voltage (V_{VCOIN}).

Phase-locked-loop with VCO

74HC/HCT406A



Phase-locked-loop with VCO

74HC/HCT4046A

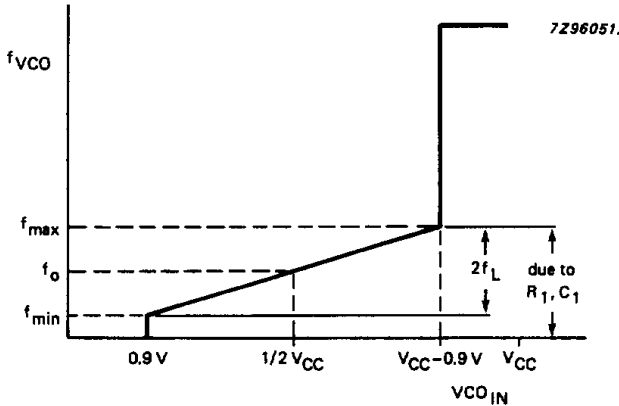
APPLICATION INFORMATION

This information is a guide for the approximation of values of external components to be used with the 74HC/HCT4046A in a phase-lock-loop system.

References should be made to Figs 29, 30 and 31 as indicated in the table.

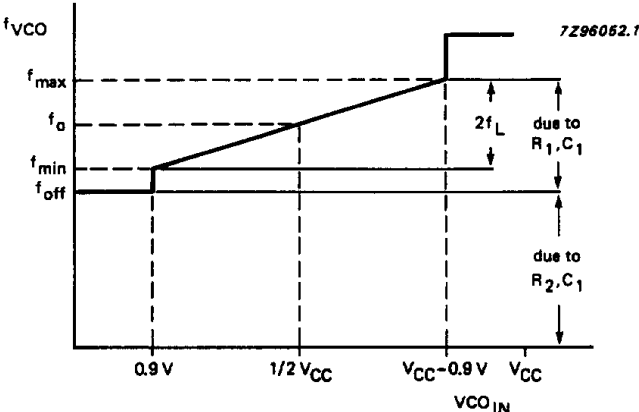
Values of the selected components should be within the following ranges:

- R1 between 3 kΩ and 300 kΩ;
- R2 between 3 kΩ and 300 kΩ;
- R1 + R2 parallel value > 2.7 kΩ;
- C1 greater than 40 pF.

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency without extra offset	PC1, PC2 or PC3	<p>VCO frequency characteristic</p> <p>With $R2 = \infty$ and $R1$ within the range $3\text{ k}\Omega < R1 < 300\text{ k}\Omega$, the characteristics of the VCO operation will be as shown in Fig.25. (Due to $R1, C1$ time constant a small offset remains when $R2 = \infty$.)</p>  <p>Fig.25 Frequency characteristic of VCO operating without offset: f_0 = centre frequency; $2f_L$ = frequency lock range.</p>
	PC1	<p>Selection of R1 and C1</p> <p>Given f_0, determine the values of $R1$ and $C1$ using Fig.29.</p>
	PC2 or PC3	<p>Given f_{max} and f_0, determine the values of $R1$ and $C1$ using Fig.29, use Fig.31 to obtain $2f_L$ and then use this to calculate f_{min}.</p>

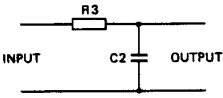
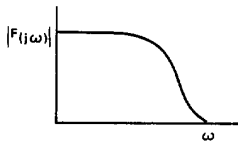
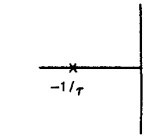
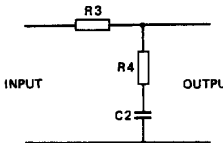
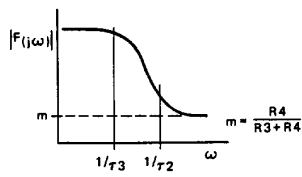
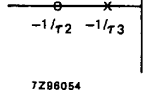
Phase-locked-loop with VCO

74HC/HCT4046A

SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
VCO frequency with extra offset	PC1, PC2 or PC3	<p>VCO frequency characteristic</p> <p>With R_1 and R_2 within the ranges $3\text{ k}\Omega < R_1 < 300\text{ k}\Omega$, $3\text{ k}\Omega < R_2 < 300\text{ k}\Omega$, the characteristics of the VCO operation will be as shown in Fig.26.</p>  <p>Fig.26 Frequency characteristic of VCO operating with offset: f_o = centre frequency; $2f_L$ = frequency lock range.</p>
	PC1, PC2 or PC3	<p>Selection of R_1, R_2 and C_1</p> <p>Given f_o and f_L, determine the value of product R_1C_1 by using Fig.31. Calculate f_{off} from the equation $f_{off} = f_o - 1.6f_L$. Obtain the values of C_1 and R_2 by using Fig.30. Calculate the value of R_1 from the value of C_1 and the product R_1C_1.</p>
PLL conditions with no signal at the SIG_{IN} input	PC1	VCO adjusts to f_o with $\phi_{DEMOUT} = 90^\circ$ and $V_{VCOIN} = 1/2 V_{CC}$ (see Fig.6).
	PC2	VCO adjusts to f_o with $\phi_{DEMOUT} = -360^\circ$ and $V_{VCOIN} = \text{min.}$ (see Fig.8).
	PC3	VCO adjusts to f_o with $\phi_{DEMOUT} = -360^\circ$ and $V_{VCOIN} = \text{min.}$ (see Fig.10).

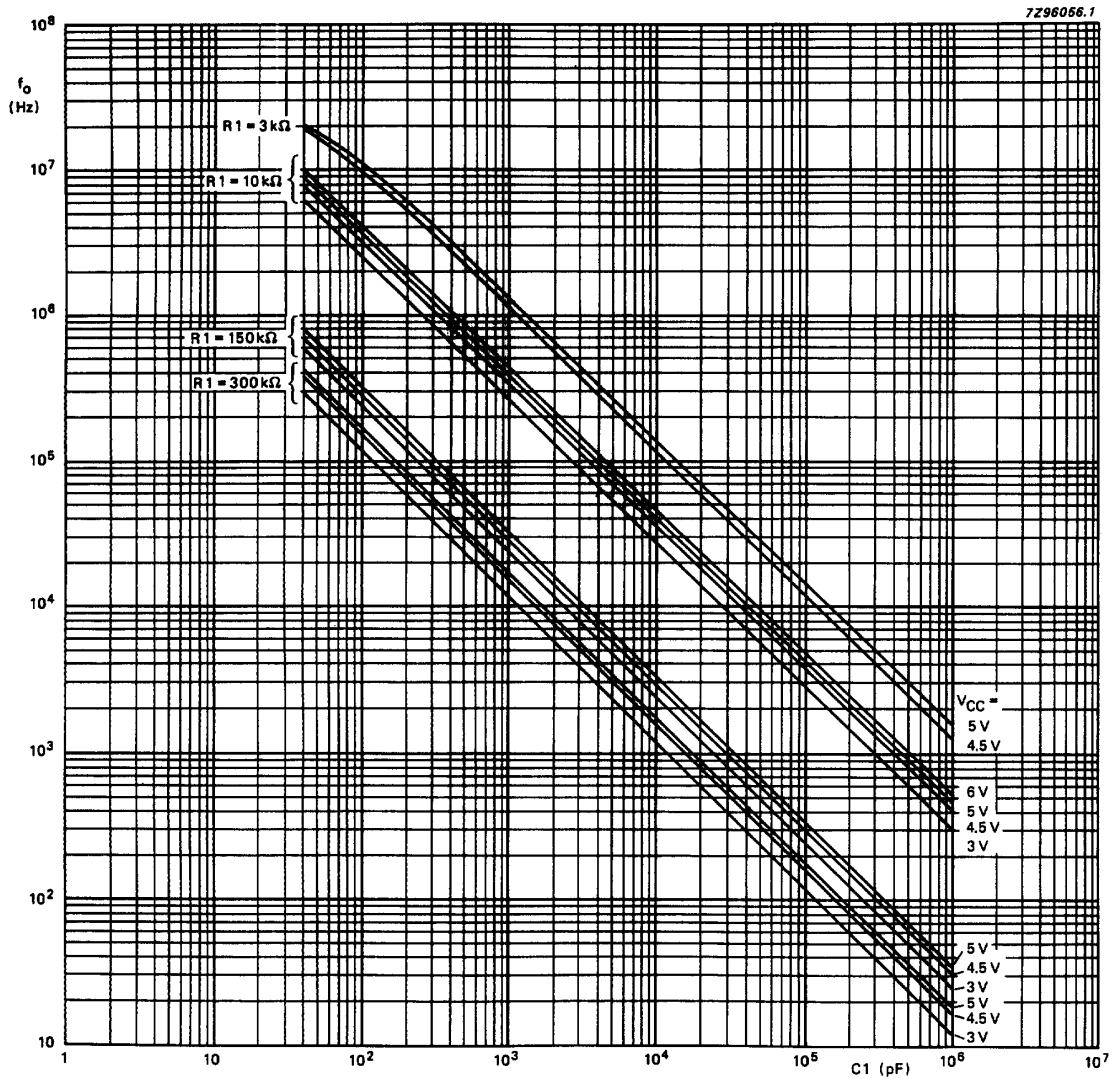
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SUBJECT	PHASE COMPARATOR	DESIGN CONSIDERATIONS
PLL frequency capture range	PC1, PC2 or PC3	<p>Loop filter component selection</p>    <p>(a) $\tau = R3 \times C2$ (b) amplitude characteristic (c) pole-zero diagram</p> <p>A small capture range ($2f_c$) is obtained if $2f_c \approx \frac{1}{\pi} \sqrt{2\pi f_L / \tau}$</p> <p>Fig. 27 Simple loop filter for PLL without offset; $R3 \geq 500 \Omega$.</p>    <p>(a) $\tau1 = R3 \times C2$; (b) amplitude characteristic (c) pole-zero diagram $\tau2 = R4 \times C2$; $\tau3 = (R3 + R4) \times C2$</p> <p>Fig.28 Simple loop filter for PLL with offset; $R3 + R4 \geq 500 \Omega$.</p>
PLL locks on harmonics at centre frequency	PC1 or PC3	yes
	PC2	no
noise rejection at signal input	PC1	high
	PC2 or PC3	low
AC ripple content when PLL is locked	PC1	$f_r = 2f_i$, large ripple content at $\phi_{\text{DEMOUT}} = 90^\circ$
	PC2	$f_r = f_i$, small ripple content at $\phi_{\text{DEMOUT}} = 0^\circ$
	PC3	$f_r = f_i$, large ripple content at $\phi_{\text{DEMOUT}} = 180^\circ$

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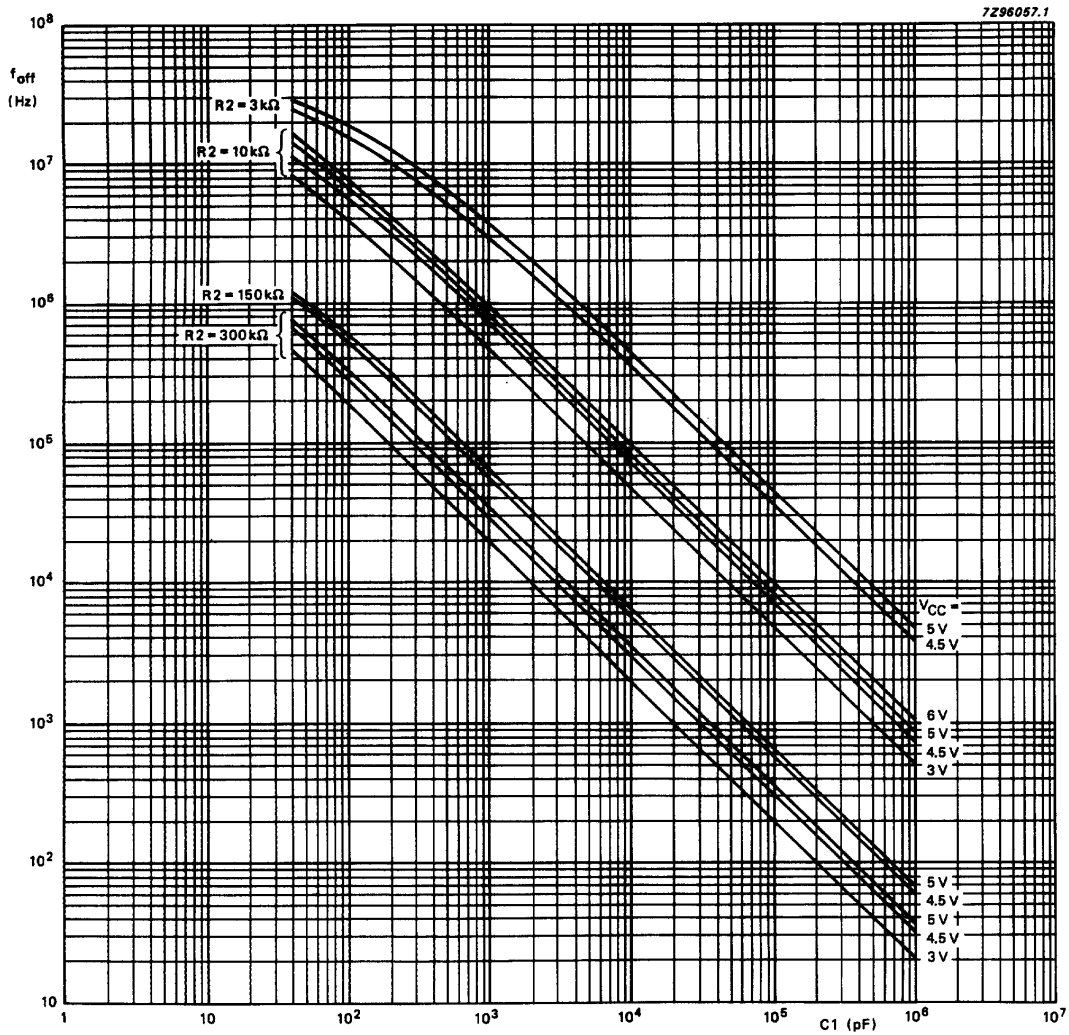


To obtain optimum VCO performance, C1 must be as small as possible but larger than 100 pF.
 Interpolation for various values of R1 can be easily calculated because a constant R1C1 product will produce almost the same VCO output frequency.

Fig.29 Typical value of VCO centre frequency (f_0) as a function of C1: $R_2 = \infty$; $V_{VCOIN} = 1/2 V_{CC}$; INH = GND; $T_{amb} = 25^\circ\text{C}$.

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To obtain optimum VCO performance, $C1$ must be as small as possible but larger than 100 pF.
 Interpolation for various values of $R2$ can be easily calculated because a constant $R2C1$ product will produce almost the same VCO output frequency.

Fig.30 Typical value of frequency offset as a function of $C1$: $R1 = \infty$; $V_{VCOIN} = 1/2 V_{CC}$; $INH = GND$; $T_{amb} = 25\text{ }^\circ\text{C}$.

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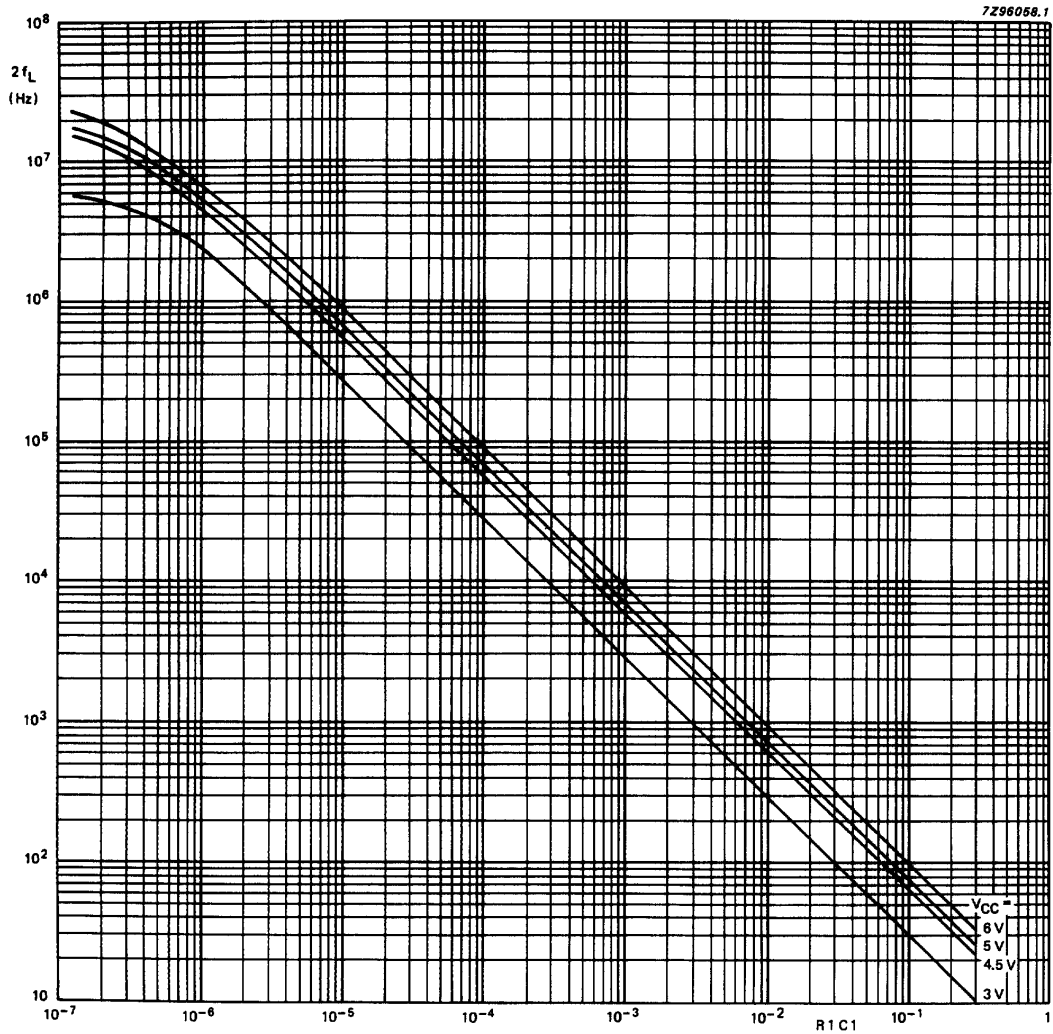


Fig.31 Typical frequency lock range ($2f_L$) versus the product $R1C1$: V_{VCOIN} range = 0.9 to $(V_{CC} - 0.9)$ V; $R2 = \infty$; VCO gain:

$$K_V = \frac{2f_L}{V_{VCOIN \text{ range}}} 2\pi \text{ (r/s/V)} .$$

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PLL design example

The frequency synthesizer, used in the design example shown in Fig.32, has the following parameters:

Output frequency: 2 MHz to 3 MHz
 frequency steps : 100 kHz
 settling time : 1 ms
 overshoot : < 20%

The open-loop gain is
 $H(s) \times G(s) = K_p \times K_f \times K_o \times K_n$.

Where:

K_p = phase comparator gain
 K_f = low-pass filter transfer gain
 K_o = K_v/s VCO gain
 K_n = 1/n divider ratio

The programmable counter ratio K_n can be found as follows:

$$N_{min.} = \frac{f_{out}}{f_{step}} = \frac{2 \text{ MHz}}{100 \text{ kHz}} = 20$$

$$N_{max.} = \frac{f_{out}}{f_{step}} = \frac{3 \text{ MHz}}{100 \text{ kHz}} = 30$$

The VCO is set by the values of R1, R2 and C1, R2 = 10 kΩ (adjustable). The values can be determined using the information in the section "DESIGN CONSIDERATIONS".

With $f_o = 2.5 \text{ MHz}$ and $f_L = 500 \text{ kHz}$ this gives the following values

($V_{CC} = 5.0 \text{ V}$):
 R1 = 10 kΩ
 R2 = 10 kΩ
 C1 = 500 pF

The VCO gain is:

$$K_v = \frac{2f_L \times 2 \times \pi}{0.9 - (V_{CC} - 0.9)}$$

$$= \frac{1 \text{ MHz}}{3.2} \times 2\pi \approx 2 \times 10^6 \text{ r/s/V}$$

The gain of the phase comparator is:

$$K_p = \frac{V_{CC}}{4 \times \pi} = 0.4 \text{ V/r.}$$

The transfer gain of the filter is given by:

$$K_f = \frac{1 + \tau_2 s}{1 + (\tau_1 + \tau_2) s}$$

Where:

$\tau_1 = R3C2$ and $\tau_2 = R4C2$.

The characteristics equation is:
 $1 + H(s) \times G(s) = 0$.

This results in:

$$s^2 + \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)} s + \frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0$$

$$\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)} = 0$$

The natural frequency ω_n is defined as follows:

$$\omega_n = \sqrt{\frac{K_p \times K_v \times K_n}{(\tau_1 + \tau_2)}}$$

and the damping value ζ is defined as follows:

$$\zeta = \frac{1}{2\omega_n} \times \frac{1 + K_p \times K_v \times K_n \times \tau_2}{(\tau_1 + \tau_2)}$$

In Fig.33 the output frequency response to a step of input frequency is shown.

The overshoot and settling time percentages are now used to determine ω_n . From Fig.33 it can be seen that the damping ratio $\zeta = 0.45$ will produce an overshoot of less than 20% and settle to within 5% at $\omega_n t = 5$. The required settling time is 1 ms.

This results in:

$$\omega_n = \frac{5}{t} = \frac{5}{0.001} = 5 \times 10^3 \text{ r/s.}$$

Rewriting the equation for natural frequency results in:

$$(\tau_1 + \tau_2) = \frac{K_p \times K_v \times K_n}{\omega_n^2}$$

The maximum overshoot occurs at $N_{max.}$:

$$(\tau_1 + \tau_2) = \frac{0.4 \times 2 \times 10^6}{5000^2 \times 30} = 0.0011 \text{ s.}$$

When C2 = 470 nF, then

$$R4 = \frac{(\tau_1 + \tau_2) \times 2 \times \omega_n \times \zeta - 1}{K_p \times K_v \times K_n \times C2} = 315 \text{ } \Omega$$

now R3 can be calculated:

$$R3 = \frac{\tau_1}{C2} - R4 = 2 \text{ k}\Omega.$$

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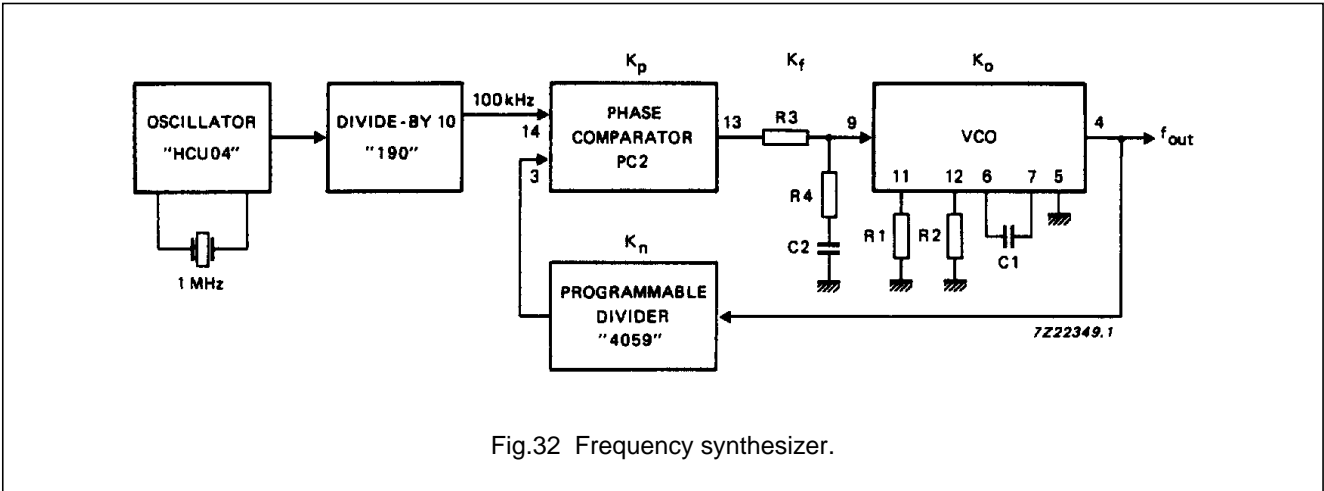


Fig.32 Frequency synthesizer.

note

For an extensive description and application example please refer to application note ordering number 9398 649 90011.

Also available a computer design program for PLL's ordering number 9398 961 10061.

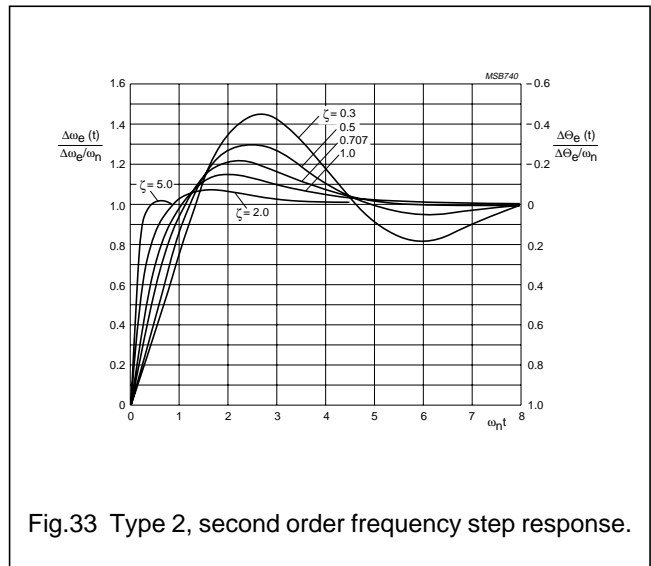


Fig.33 Type 2, second order frequency step response.

Since the output frequency is proportional to the VCO control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 9 of the VCO. The average frequency response, as calculated by the Laplace method, is found experimentally by smoothing this voltage at pin 9 with a simple RC filter, whose time constant is long compared to the phase detector sampling rate but short compared to the PLL response time.

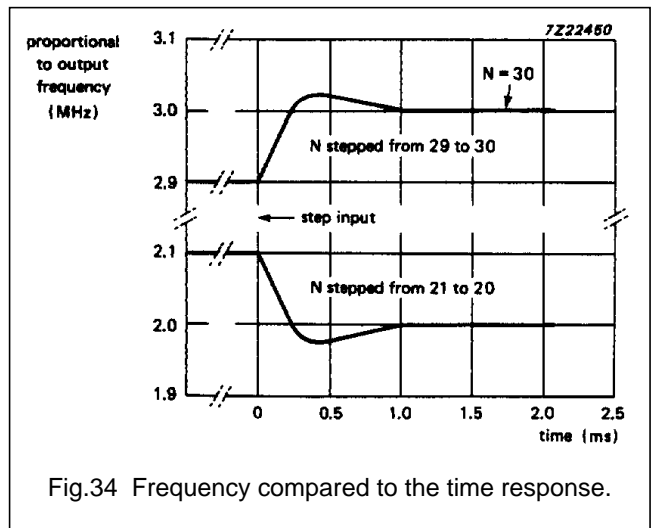


Fig.34 Frequency compared to the time response.

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SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our "IC Package Databook" (order code 9398 652 90011).

DIP

SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

SO, SSOP and TSSOP

REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO, SSOP and TSSOP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method.

Typical reflow temperatures range from 215 to 250 °C. Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

WAVE SOLDERING

Wave soldering can be used for all SO packages. Wave soldering is **not** recommended for SSOP and TSSOP packages, because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering is used - **and cannot be avoided for SSOP and TSSOP packages** - the following conditions must be observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow and must incorporate solder thieves at the downstream end.

Even with these conditions:

- **Only consider wave soldering SSOP packages that have a body width of 4.4 mm, that is SSOP16 (SOT369-1) or SSOP20 (SOT266-1).**
- **Do not consider wave soldering TSSOP packages with 48 leads or more, that is TSSOP48 (SOT362-1) and TSSOP56 (SOT364-1).**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

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DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

LIFE SUPPORT APPLICATIONS

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